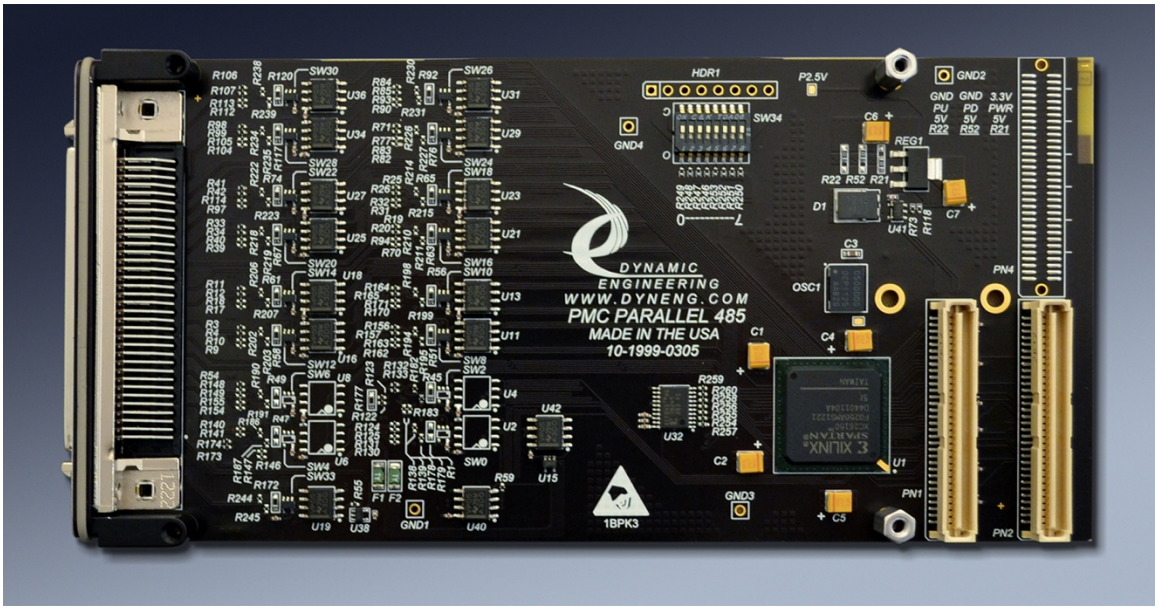
DYNAMIC ENGINEERING
150 DuBois St. Suite B/C, Santa Cruz, CA 95060
831-457-8891
sales@dyneng.com https://www.dyneng.com
Est. 1988

User Manual

PMC-PARALLEL-485

Digital Parallel Interface
PMC Module



Revision 05p1 8/9/22
Corresponding Hardware: Revision 05
10-1999-0305

PMC-PARALLEL-485

Digital Parallel Interface
PMC Module

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

.

Table of Contents

List of Figures

Product Description

PMC-PARALLEL-485 is part of the PCI Mezzanine Card [PMC] family of modular I/O components. PMC-PARALLEL-485 provides 32 differential IO lines in one PMC position. The IO lines are resistor isolated with options to connect to a 68-pin SCSI connector and/or the backplane connector. In addition, a bi-directional clock and clock enable differential pair are provided at the front panel.

Originally released in 1999 and still available. A few updates to keep in production ⇔ original FPGA was a Spartan 40. Currently using a Spartan II device. For similar models with more capability see PMC-BiSerial-VI.

Each of the 32 differential pairs is programmable to be an input or an output. The lower 4 bits [3-0] are individually programmable. The remaining bits are programmed on a nibble basis. Input, Output, Termination active or disabled.

The IO are available as inputs in two forms. The data can be read directly without filtering, or from a data latch which captures any detected 'hi' condition. The data can be selectively inverted and masked prior to the latch function. The data latches can be programmed to respond to a rising or falling edge, or simply to the voltage level of the signal. The direct read data is unaffected by the inversion, filtering, and masking. The output lines are driven from the output register.

The 485 transceivers are selectively enabled for transmitting and always enabled for receiving. Separate input and output lines between the FPGA and the transceivers allow for local loop-back if the transceivers are enabled to transmit.

Each differential pair incorporates a parallel termination resistor with analog switch. The switches are programmed to activate the termination. For cable terminated environments the analog switches can be programmed to be disabled. The standard resistor value is 100 ohms. Alternate values can be installed. Contact Dynamic Engineering for this option.

A dip switch with eight “user bits” are supplied for user configuration control and other user purposes. The same register also contains the Revision fields [Major, Minor].

A clock generator is provided which can be referenced to an external source, the local oscillator or the PCI clock. The generator has a programmable divider. The clock can be selected to be used for the output data to gate to a particular frequency or to use an external clock and enable to control the output.

All configuration registers support read and write operations for maximum software convenience. LW operations are supported (please refer to the memory map).

PMC-PARALLEL-485 conforms to the PMC standard. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

Theory of Operation

PMC-PARALLEL-485 is designed for the purpose of transferring data from one point to another with a parallel protocol.

PMC-PARALLEL-485 features a Xilinx FPGA and 34 differential transceivers. Transceivers can be programmed to be drivers or receivers. Transceivers can be RS-485 [RS-422 compatible] or LVDS.

Terminations can be programmed to be active or disabled. The controls are individual for IO 0-3 and by groups of four IO for IO 4-31. The clock and clock enable have a common direction control. The FPGA contains the PCI interface and control required for the parallel interface.

The PCI interface is achieved with the Dynamic Engineering PCI Core design. Specialized versions are in use for Spartan II and Spartan IV architectures.

Three registers are used to interact with the basic data interface. The output data register [pmc_par485_dataout] is connected to the driver side of the '485 transceiver. The input register [pmc_par485_datain] is read-able from the host and is connected to the receive side of the transceiver. The direction register [pmc_par485_dir_term] has a bit corresponding to each IO or nibble group which controls the direction of each transceiver. The direction controls default to read. The terminations are programmed through the same register.

If set to drive the bus the value driven corresponds to the bit in the output data register. The output data register is read-writeable, since the register is independent of the bus, the data read will always match the data written allowing read-modify-write operations. The separate input register provides access to the IO bus side of the drivers. The data read will reflect the state of the bus, and not necessarily the state of the on-board drivers. Please see the connector definitions and register descriptions for more detail.

The input data is registered and clocked with the PCI bus clock. The data is available "as-is" via the "datain" register. A filtered version of the data is available from the "datain_lat" register. Each data input line has three corresponding filter control bits one in each of the "pol", "edge/level", and "mask" registers. The "pol" register controls inversion of the input data. The "edge/level" register controls whether the latch responds to a rising or falling edge (controlled by the "pol" setting) or the voltage level of the signal. The "mask" register controls which bits can be latched by the data latch. Once a filtered data bit is captured the data is held in the latch until cleared. The latch is cleared on a bit selectable basis by a write to the latch. The bits that are written as ones will be cleared until new data is detected.

The onboard clock generator can utilize an external clock, the PCI clock or the onboard reference oscillator [optional] as a clock source. Further the generator can be programmed to divide the reference down to provide a useful frequency. The "base" control register controls the operation of the generator, the clock enable and external clock direction.

The interrupt sources correspond to the data bits that are selected to be latched. The interrupt state is available masked and unmasked in the "stat" register to allow polling and interrupt priority processing. In addition, an extra signal [force int] is supplied to allow software generated interrupts for development and debugging purposes. The master interrupt enable, and force interrupt bits are also located in the "base" control register.

Programming

Programming PMC-PARALLEL-485 requires the ability to read and write data in the host's PMC space. The base address is determined by the host. This documentation refers to the BAR address of the PMC-Parallel-485, as the base address.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

PMC-Parallel-485 has a VendorID of 0x10EE and a CardID of 0x0009. The current PCI revision is 0x01. Your driver can use the configuration information to identify PMC-Parallel-485 during initialization in systems where address spaces are allocated dynamically.

Address Map

Function	Offset	Function
// PMC relative addresses //		
#define pmc_par485_base	0x00	// clock and interrupt control
#define pmc_par485_stat	0x04	// interrupt status
#define pmc_par485_eg_lvl	0x08	// data latch edge or level control
#define pmc_par485_mask	0x0C	// data latch mask register
#define pmc_par485_pol	0x10	// data in polarity selection reg.
#define pmc_par485_dir_term	0x14	// direction and termination reg.
#define pmc_par485_dataout	0x18	// output data register
#define pmc_par485_datain	0x24	// data input register
#define pmc_par485_datain_lat	0x28	// data input latched register
#define pmc_par485_sw	0x44	// read the user dip switch setting

FIGURE 1 PMC-PARALLEL-485 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within PMC-Parallel-485. The addresses are all offsets from a base address.

Register Definitions

pmc_par485_base

[$00] parallel-485 Base Control Port read/write

BASE CONTROL REGISTER

DATA BIT	DESCRIPTION
31-20	Spare
19	Master Interrupt Enable
18	Force Interrupt
17	Enable Select
16	Clock Enable
15	External Clock Direction
14-13	Clock Pre-Selector
12	Clock Post-Selector
11-0	Divisor

FIGURE 2 PMC-PARALLEL-485 BASE CONTROL BIT MAP

The PS [pre-selector] bits are used to select from the clock sources.
00 = '0' no clock
01 = Oscillator – (Optional - Frequency selectable)
10 = External Clock - received from an RS 485 differential pair
11 = PCI Clock

Divisor [11-0] are the clock divisor select bits. The clock source is divided by a counter and the select bits pick which clock is used to drive the divider network and the clock output. The reference clock for the counter is selected with the CLK Pre-Selector. The output frequency is {reference / [2(n+1)]}. N≥1. The reference oscillator frequency is user selectable. The counter divides by N+1 due to counting from 0 ->n before rolling over. The output is then divided by two to produce a square wave output.

Post Selector when '1' sets clock out to the divided clock, when '0' sets clock out to pre-selector referenced clock.

Please note that the 485 buffers are rated for 50 MHz.
The LVDS buffers are rated at 200 MHz.

The external clock direction bit controls the direction of the external clock and clock enable drivers. When this bit is a '1' these drivers are configured as outputs, otherwise they are inputs.

The clock enable bit is the internal source for enabling the output clock. When this bit is a '1' the clock is enabled except when the external clock enable is being used.

The enable select bit selects the enable source when the external clock drivers are configured as inputs. When this bit is a '1' the external enable input is used to enable the clock, otherwise the clock enable bit performs this function (see above).

The force interrupt bit is used to generate an interrupt condition regardless of input data levels.

The master interrupt enable bit enables the interrupt onto the PCI bus. When this bit is a '1' and an interrupt condition exists, a system interrupt is generated.

pmc_par485_stat

[$04] parallel-485 Status Port read only

STATUS REGISTER

DATA BIT	DESCRIPTION
31-4	
3	Virtual Filtered interrupt bit
2	Force Int
1	Interrupt Out
0	Interrupt Status

FIGURE 3 PMC-PARALLEL-485 STATUS BIT MAP

The Status register provides a read-only port for interrupt status.

The interrupt status bit, when '1', indicates that an interrupt condition exists, either from input data conditions, or the force interrupt bit.

The interrupt out bit, when '1', indicates that a system interrupt is asserted. This occurs when both an interrupt condition exists and the master enable bit is asserted.

Force Int is a copy of the Force interrupt control bit to allow the ISR to read this potential source from the status register.

The virtual bit is a software bit reserved for the ISR to set if any of the filtered interrupt bits are set. This allows the User application to respond to the interrupt with one fewer reads. Not all OS implementations will take advantage of this – see the SW manual for

details.

pmc_par485_eg_lvl

[$08] parallel-485 Edge/Level Control Register Port read/write

CONTROL REGISTER EDGE/LEVEL	
DATA BIT	**DESCRIPTION**
31-0	Edge Enable

FIGURE 4 PMC-PARALLEL-485 EDGE/LEVEL CONTROL BIT MAP

When an edge enable bit is a '1', the corresponding data bit will be latched when an edge occurs, provided its mask bit is enabled. If the bit is a '0', the level of the signal is used. The polarity of the edge or level depends on the state of the corresponding bit in the polarity register.

pmc_par485_mask

[$0C] parallel-485 Mask Port read/write

CONTROL REGISTER MASK	
DATA BIT	**DESCRIPTION**
31-0	1 = enable, 0 = mask off for data input latch

FIGURE 5 PMC-PARALLEL-485 MASK CONTROL BIT MAP

If an input bit is desired to be monitored then the corresponding mask bit should be set to '1'. To keep an input bit from being active, set the corresponding bit to '0'.

pmc_par485_**pol**

[$10] parallel-485 Polarity Port read/write

CONTROL REGISTER POLARITY	
DATA BIT	**DESCRIPTION**
31-0	1 = invert, 0 = normal

FIGURE 6 PMC-PARALLEL-485 POLARITY CONTROL BIT MAP

If an input bit is active low then the corresponding polarity bit should be set to '1'. The data input latch will capture the level of a signal. Active low signals should be inverted to capture the active state. If the corresponding edge enable bit is set, then a '1' indicates a falling edge and a '0' indicates a rising edge.

pmc_par485_dir_**term**

[$14] parallel-485 direction and termination Port read/write

CONTROL REGISTER DIR_TERM	
DATA BIT	**DESCRIPTION**
10-0	DIRection 10-0 0 = tristate, 1 = drive
26-16	TERMination 10-0 1 = terminated

FIGURE 7 PMC-PARALLEL-485 DIRECTION TERMINATION CONTROL BIT MAP

The direction for each of the 32 differential pairs is controlled through this port. The port defaults to ‘0’ which corresponds to tri-stating the drivers. The output and input pins are separated and independently connected to the FPGA to allow loop-back testing. The input side is always active.

CONTROL	CORRESPONDING IO BIT(S)
DIR_0..3	IO_0..3.
DIR4	IO_4..7
DIR5	IO_8..11
DIR6	IO_12..15
DIR7	IO_16..19
DIR8	IO_20..23
DIR9	IO_24..27
DIR10	IO_28..31

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated. In some systems it will make sense to terminate the lines in the cable, and in cases it will make sense to use the onboard terminations.

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..3	IO_0..3.
TERM4	IO_4..7
TERM5	IO_8..11
TERM6	IO_12..15
TERM7	IO_16..19
TERM8	IO_20..23
TERM9	IO_24..27
TERM10	IO_28..31

pmc_par485_dataout

[$18] parallel-485 Write Port read/write

CONTROL REGISTER DATA OUT	
DATA BIT	**DESCRIPTION**
31-0	IO31-IO0

FIGURE 8 PMC-PARALLEL-485 DATAOUT BIT MAP

The 32 bits are written through this port. The port is on the single ended side of the transceivers. The data read will match the data written to this port because the Xilinx internal register is being read.

The data written to this port is double-clocked with the inverted output clock, therefore this data will appear on the output drivers within two clock periods of being written, provided the clock is enabled.

pmc_par485_datain

[$24] parallel-485 data input read only

DATA INPUT PORT	
DATA BIT	**DESCRIPTION**
31-0	Value currently on data input lines

FIGURE 9 PMC-PARALLEL-485 DATA IN BIT MAP

The "natural" data from the input port is available on this port. The data input lines are continuously sampled with Xilinx input flip-flops at the PCI clock rate. When a read occurs the value on the flip-flops is returned to the host.

pmc_par485**_datain_lat**

[$28] parallel-485 data input latch/clear latch read/write

LATCHED DATA INPUT PORT	
DATA BIT	**DESCRIPTION**
31-0	Value in input data latch

FIGURE 10 PMC-PARALLEL-485 DATA IN LATCHED BIT MAP

The filtered and captured data is available from this port. The data is cleared by writing a '1' to the bit to be cleared. See the Polarity, Edge/Level and Mask registers for more details on the filtering capabilities.

pmc_par485_sw

[$44] Parallel-485 Switch Read Port read only

USER SWITCH PORT	
DATA BIT	**DESCRIPTION**
23-16	RevMaj
15-8	RevMin
7-0	SW7-0

FIGURE 11 PMC-PARALLEL-485 SWITCH READ BIT MAP

The Switch Read Port reports the current value of the dip switch, plus the Major and Minor revision fields.

The switches allow custom configurations to be defined by the user and for the software to “know” how to configure the read/write capabilities of each IO line.

Revision Major is changed when large changes happen to the design, new features of merit etc. Current Revision Major is 0x01.

Revision Minor is changed with each update no matter how minor [once released]. Current is 0x02.

Major.Minor history
1p2 8/2/22 re-released with Major and Minor revision fields, added status bits, other minor clean-up. In support of Win10 driver / user application development.

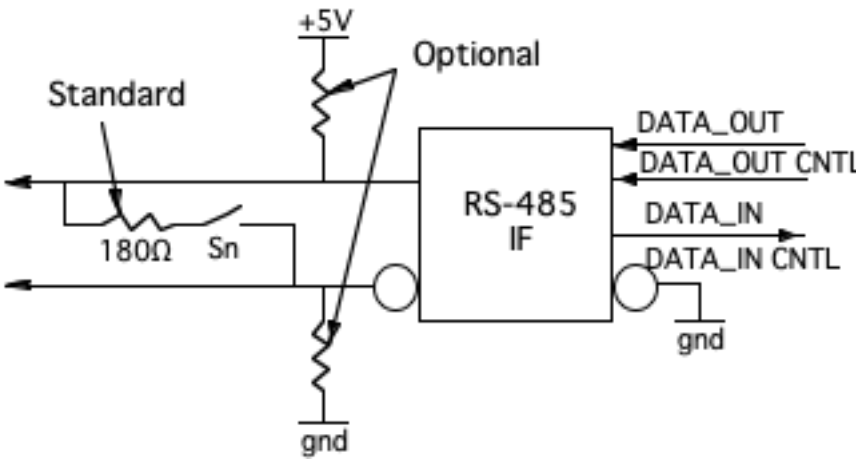


FIGURE 12 PMC-PARALLEL-485 TERMINATION

The PMC-PARALLEL-485 design layout provides for a variety of termination options. The standard programmable termination is 100Ω parallel. Factory options include:
1) different parallel termination values [for example 180 ohms]
2) pull-up / pull-down resistors
3) Fused 3.3V reference
4) ground references
5) special circuit which receives one differential pair which is then driven out on two differential pairs and one open drain circuit.

The first two options are available on all IO pairs. The 3rd, 4th, and 5th options are restricted to certain pins. Please refer to the "Alternate" pin definitions in the next section of this document. Please contact Dynamic Engineering if an alternate configuration is needed for your project.

Loop-Back

PMC-Parallel-485 has options for Front and Rear Panel IO. Loop-back testing is performed during the ATP. The tables show the interconnections using a modified HDEterm68, SCSI cable and either front panel or rear panel IO connections. With rear IO the carrier routes the connections from Pn4 to the SCSI connector on the rear of the carrier. The HDEterm68 connections are modified accordingly.

Front Panel IO connections on HDEterm68

From	To	Signals	
1	3	EXT_CLK_ENP	IO_0P
35	37	EXT_CLK_ENN	IO_0N
2	4	EXT_CLKP	IO_1P
36	38	EXT_CLKN	IO_1N
3	19	IO_0P	IO_16P
37	53	IO_0N	IO_16N
4	20	IO_1P	IO_17P
38	54	IO_1N	IO_17N
5	21	IO_2P	IO_18P
39	55	IO_2N	IO_18N
6	22	IO_3P	IO_19P
40	56	IO_3N	IO_19N
7	23	IO_4P	IO_20P
41	57	IO_4N	IO_20N
8	24	IO_5P	IO_21P
42	58	IO_5N	IO_21N
9	25	IO_6P	IO_22P
43	59	IO_6N	IO_22N
10	26	IO_7P	IO_23P
44	60	IO_7N	IO_23N
11	27	IO_8P	IO_24P
45	61	IO_8N	IO_24N
12	28	IO_9P	IO_25P
46	62	IO_9N	IO_25N
13	29	IO_10P	IO_26P
47	63	IO_10N	IO_26N
14	30	IO_11P	IO_27P
48	64	IO_11N	IO_27N
15	31	IO_12P	IO_28P
49	65	IO_12N	IO_28N
16	32	IO_13P	IO_29P
50	66	IO_13N	IO_29N
17	33	IO_14P	IO_30P
51	67	IO_14N	IO_30N
18	34	IO_15P	IO_31P
52	68	IO_15N	IO_31N

PN4 IO connections on HDEterm68 using PCIBPMC

Pn4		SCSI/HDEterm68			
From	To	From	To	From	To
1	33	1	17	IO_0P	IO_16P
2	34	35	51	IO_0N	IO_16N
3	35	2	18	IO_1P	IO_17P
4	36	36	52	IO_1N	IO_17N
5	37	3	19	IO_2P	IO_18P
6	38	37	53	IO_2N	IO_18N
7	39	4	20	IO_3P	IO_19P
8	40	38	54	IO_3N	IO_19N
9	41	5	21	IO_4P	IO_20P
10	42	39	55	IO_4N	IO_20N
11	43	6	22	IO_5P	IO_21P
12	44	40	56	IO_5N	IO_21N
13	45	7	23	IO_6P	IO_22P
14	46	41	57	IO_6N	IO_22N
15	47	8	24	IO_7P	IO_23P
16	48	42	58	IO_7N	IO_23N
17	49	9	25	IO_8P	IO_24P
18	50	43	59	IO_8N	IO_24N
19	51	10	26	IO_9P	IO_25P
20	52	44	60	IO_9N	IO_25N
21	53	11	27	IO_10P	IO_26P
22	54	45	61	IO_10N	IO_26N
23	55	12	28	IO_11P	IO_27P
24	56	46	62	IO_11N	IO_27N
25	57	13	29	IO_12P	IO_28P
26	58	47	63	IO_12N	IO_28N
27	59	14	30	IO_13P	IO_29P
28	60	48	64	IO_13N	IO_29N
29	61	15	31	IO_14P	IO_30P
30	62	49	65	IO_14N	IO_30N
31	63	16	32	IO_15P	IO_31P
32	64	50	66	IO_15N	IO_31N

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 13 PMC-PARALLEL-485 PN1 INTERFACE

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-PARALLEL-485. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 14 PMC-PARALLEL-485 PN2 INTERFACE

PMC Module Front Panel IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
IO_0P	IO_0N	3	37
IO_1P	IO_1N	4	38
IO_2P	IO_2N	5	39
IO_3P	IO_3N	6	40
IO_4P	IO_4N	7	41
IO_5P	IO_5N	8	42
IO_6P	IO_6N	9	43
IO_7P	IO_7N	10	44
IO_8P	IO_8N	11	45
IO_9P	IO_9N	12	46
IO_10P	IO_10N	13	47
IO_11P	IO_11N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_19N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 15 PMC-PARALLEL-485 FRONT PANEL INTERFACE STANDARD

PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485 and routed to Pn4. Also see the User Manual for your carrier board for more information.

IO_0P	IO_0N	1	2
IO_1P	IO_1N	3	4
IO_2P	IO_2N	5	6
IO_3P	IO_3N	7	8
IO_4P	IO_4N	9	10
IO_5P-	IO_5N	11	12
IO_6P-	IO_6N	13	14
IO_7P-	IO_7N	15	16
IO_8P-	IO_8N	17	18
IO_9P-	IO_9N	19	20
IO_10P-	IO_10N	21	22
IO_11P-	IO_11N	23	24
IO_12P-	IO_12N	25	26
IO_13P-	IO_13N	27	28
IO_14P-	IO_14N	29	30
IO_15P-	IO_15N	31	32
IO_16P	IO_16N	33	34
IO_17P	IO_17N	35	36
IO_18P	IO_18N	37	38
IO_19P	IO_19N	39	40
IO_20P-	IO_20N	41	42
IO_21P-	IO_21N	43	44
IO_22P-	IO_22N	45	46
IO_23P-	IO_23N	47	48
IO_24P-	IO_24N	49	50
IO_25P	IO_25N	51	52
IO_26P	IO_26N	53	54
IO_27P	IO_27N	55	56
IO_28P	IO_28N	57	58
IO_29P-	IO_29N	59	60
IO_30P-	IO_30N	61	62
IO_31P-	IO_31N	63	64

FIGURE 16 PMC-PARALLEL-485 PN4 INTERFACE STANDARD

PMC Module Front Panel IO Alternate Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485. These are the alternate pin definitions. Also see the User Manual for your carrier board for more information.

EXT_CLK_ENP	EXT_CLK_ENN	1	35
EXT_CLKP	EXT_CLKN	2	36
3.3V	3.3V	3	37
gnd	gnd	4	38
gnd	gnd	5	39
RSTINP	RSTINN	6	40
RSTOUT1P	RSTOUT1N	7	41
RSTOUT2P	RSTOUT2N	8	42
RESET*	UNUSED	9	43
IO_7P	IO_7N	10	44
CLK1P	CLK1N	11	45
RST1P	RST1N	12	46
CLK2P	CLK2N	13	47
RST2P	RST2N	14	48
IO_12P	IO_12N	15	49
IO_13P	IO_13N	16	50
IO_14P	IO_14N	17	51
IO_15P	IO_15N	18	52
IO_16P	IO_16N	19	53
IO_17P	IO_17N	20	54
IO_18P	IO_18N	21	55
IO_19P	IO_19N	22	56
IO_20P	IO_20N	23	57
IO_21P	IO_21N	24	58
IO_22P	IO_22N	25	59
IO_23P	IO_23N	26	60
IO_24P	IO_24N	27	61
IO_25P	IO_25N	28	62
IO_26P	IO_26N	29	63
IO_27P	IO_27N	30	64
IO_28P	IO_28N	31	65
IO_29P	IO_29N	32	66
IO_30P	IO_30N	33	67
IO_31P	IO_31N	34	68

FIGURE 17 PMC-PARALLEL-485 FRONT PANEL INTERFACE ALTERNATE

PMC Module Backplane IO Alternate Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-Parallel_485 and routed to Pn4. These are the alternate pin assignments. Also see the User Manual for your carrier board for more information.

3.3V	3.3V	1	2
GND	GND	3	4
GND	GND	5	6
RSTINP	RSTINN	7	8
RSTOUT1P	RSTOUT1N	9	10
RSTOUT2P	RSTOUT2N	11	12
RESET*	UNUSED	13	14
IO_7P	IO_7N	15	16
CLK1P	CLK1N	17	18
RST1P	RST1N	19	20
CLK2P	CLK2N	21	22
RST2P	RST2N	23	24
IO_12P	IO_12N	25	26
IO_13P	IO_13N	27	28
IO_14P	IO_14N	29	30
IO_15P	IO_15N	31	32
IO_16P	IO_16N	33	34
IO_17P	IO_17N	35	36
IO_18P	IO_18N	37	38
IO_19P	IO_19N	39	40
IO_20P	IO_20N	41	42
IO_21P	IO_21N	43	44
IO_22P	IO_22N	45	46
IO_23P	IO_23N	47	48
IO_24P	IO_24N	49	50
IO_25P	IO_25N	51	52
IO_26P	IO_26N	53	54
IO_27P	IO_27N	55	56
IO_28P	IO_28N	57	58
IO_29P	IO_29N	59	60
IO_30P	IO_30N	61	62
IO_31P	IO_31N	63	64

FIGURE 18 PMC-PARALLEL-485 PN4 INTERFACE ALTERNATE

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a lowcost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC Parallel 485 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC BiSerial-II does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the PMC Parallel 485 pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68-screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68 **[https://www.dyneng.com/HDEterm68.html]**

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages**.**

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The Parallel-485 is constructed out of 0.062 inch thick high temperature ROHS compatible FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with the connectors and front panel. If more security against vibration is required the stand-offs can be secured against the carrier.

The PMC Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, taking into account the thickness and area of the PMC. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-PARALLEL-485 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St.
Suite B/C
Santa Cruz, CA 95060
831-457-8891
E-Mail Address support@dyneng.com

Specifications

Logic Interface:	PMC Logic Interface [PCI 33/32]
Digital Parallel IO:	32 differential IO channels. Each with direction control. Additional External Clock input and External Clock Enable.
CLK rates supported:	Multiple rate divisors supplied based on PCI, External, or board mounted oscillator.
Software Interface:	Control Registers, IO registers, IO Read-Back registers
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW aligned
Access Time:	1 PCI wait state
Interrupt:	Edge or Level Detect on any of the 32 IO lines
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 Pin SCSI III connector via front panel User IO routed to Pn4
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{O}C for uniform heat across PMC
Power:	Typical 300 mA @ 5V

Order Information

standard temperature range -40-85ºC

PMC-PARALLEL-485	PMC Module with 32 differential IO plus External clock and External Clock Enable. Standard with RS-485 IO at the bezel. https://www.dyneng.com/PMC-Parallel-485.html
-LVDS	Switch IO to LVDS transceivers.
-RIO	Switch to Pn4 IO instead of Bezel IO [SCSI]
-FRP	Both Bezel and Rear IO installed.
-CC	Add conformal coating
-ROHS	Add ROHS processing
HDEterm68	https://www.dyneng.com/HDEterm68.html SCSI to Screw Terminal Adapter for signal breakout. Can be used for loop-back.
SCSI Cable	https://www.dyneng.com/HDEcabl68.html Interconnect bezel on PMC-Parallel-485 with HDEterm68. Available in several lengths and options for latch block or screw terminal retention.